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WHAT IS CLAIMED IS:

1.   A register file comprising:

a plurality of input ports each for receiving therethrough a write data and having a priority order specified among said input ports; and

a plurality of registers each for storing therein said write data based·
5 on a write address, each of said registers including an input port selector and a data storage for storing an output from said input port selector, said input port selector including a combinational circuit including a plurality of first AND gates each corresponding to one of said input ports and a first OR gate for generating a logical sum of outputs from said first AND gates,
10 wherein:

each of said first AND gates in one of said input port selector receives a write instruction signal for specifying whether or not write data input through a corresponding one of said input ports is to be stored in a corresponding one of said registers, and generates a logical product of said
15 write data and said write instruction signal and an inverted signal of each of said write instruction signals received through said input ports each having a higher priority order compared to said input port corresponding to said one of said input port selector.

2.   The register file according to claim 1, further comprising a plurality of output ports and a plurality of output port selectors each for corresponding to one of said output ports, wherein each of output port selectors includes second AND gates each disposed corresponding to one

of said registers for generating a logical product of data stored in a corresponding one of said registers and an activating signal assuming a high level upon selection of said corresponding one of said register and a second OR gate generating a logical sum of outputs from said first AND gates.

3.   The register file according to claim 1, wherein said data storage includes a synchronous D-FF including a master latch for latching an output from said first OR gate, and a slave latch for receiving data from said master latch.

4.   The register file according to claim 1, wherein said write instruction signal is generated by a logical product of a decoded signal decoded from said write address to have bits in number corresponding to the number of said registers and a write enable signal specifying whether or not each of said input ports is allowed to write data.

5.   A register file comprising:

a plurality of registers;

a plurality of output ports each for delivering therethrough data stored in one of said registers specified by a read address;

a plurality of read data selectors each corresponding to one of said output ports, each of said read data selectors including AND gates in number corresponding to said a number of registers and an OR gate generating a logical sum of outputs from said AND gates, each of said

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AND gates generating a logical product of data stored in a corresponding
10   one of said registers and an activating signal which assumes a high level
when said corresponding one said registers is specified.

6.   A method for designing the register file as defined in claim 5,
comprising the step of describing each of said read data selectors in a
design description so that said each of said read data selectors is
implemented by a combinational circuit including said AND gates and said
5   OR gate.